Amendments to the Drawing Figures:

The attached drawing sheets include proposed changes to FIGs. 1 and 4 and replace the original sheets including FIGs. 1 and 4.

Attachment: Replacement Sheets.

REMARKS/DISCUSSION OF ISSUES

By this Amendment, Applicants cancel claims 3, 11, 12 and 14 without disclaimer of the underlying subject matter or prejudice against subsequent future prosecution. Applicants also amend FIGs. 1 and 4 and claims 1, 13 and 17, and add new claims 24-25. Accordingly, claims 1-2, 4-8, 13, 15-18 and 20-25 are pending in the application.

Reexamination and reconsideration are respectfully requested in view of the following Remarks.

OBJECTIONS TO DRAWINGS

By this Amendment, Applicants cancel claims 11-12 and 15, and submit new drawing sheets for FIGs. 1 and 4, with all of the boxes shown therein labeled.

Accordingly, Applicants respectfully respect that the objections to the drawings be withdrawn.

CLAIM OBJECTIONS

By this Amendment, Applicants amend claim 1.

Applicants respectfully submit that this amendment overcomes the objection to claim 1.

Accordingly, Applicants respectfully respect that the objection to claim 1 be withdrawn.

35 U.S.C. § 103

The Office Action rejects: claims 1, 5-8, 13, 15-16 and 20-23 under 35 U.S.C. § 103 over Fleck et al. U.S. Patent 6,434,689 ("Fleck") in view of Roussakov U.S. Patent 6,092,174 ("Roussakov"); claim 2 under 35 U.S.C. § 103 over Fleck in view of Roussakov and further in view of Miyamori et al. "REMARC: Reconfigurable multimedia array coprocessor" ("Miyamori"); and claims 4 and 17-18 under 35 U.S.C. § 103 over Fleck in view of Roussakov and further in view of Barat et al.

"*Reconfigurable instruction set processor: An implementation platform for interactive multimedia applications*" ("Barat").

Applicants respectfully submit that all of the claims 1-2, 4-8, 13, 15-18 and 20-25 are patentable over the cited art for at least the following reasons.

Claim 1

Among other things, the coprocessor of claim 1 includes a two-dimensional array of processing cells and an interface module comprising a plurality of input/output pads for the coprocessor, a plurality of border cells disposed along an outside of the two-dimensional array, each border cell being connected to a corresponding one of the periphery cells, each border cell including a buffer, and a crossbar network for reconfigurably connecting each of the I/O pads to one of the border cells.

Applicants respectfully submit that neither Fleck, nor Roussakov, nor any combination thereof discloses or suggests a coprocessor including this combination of features.

Accordingly, for at least these reasons, Applicants respectfully submit that claim 1 is patentable over the cited art.

Claims 5-8 and 21-23

Claims 5-8 and 21-23 depend from claim 1 and are deemed patentable for at least the reasons set forth above with respect to claim 1.

Claims 2 and 4

Claims 2 and 4 depend from claim 1. Applicants respectfully submit that Miyamori and Barat do not remedy the shortcomings of Fleck and Roussakov as set forth above with respect to claim 1. Accordingly, claims 2 and 4 are deemed patentable for at least the reasons set forth above with respect to claim 1.

Claim 13

Among other things, the functional unit of claim 13 includes a mechanism external to the two-dimensional array for reconfiguring a plurality of intra-processor information paths to the array to respective cells on a periphery of the array.

The Office Action cites elements 17 and 18 of Roussakov as supposedly disclosing a mechanism for reconfiguring a plurality of intra-processor information paths to the array to respective cells on a periphery of the array. The Office Action states that the "broadest reasonable interpretation" is "reconfiguring information paths within the processing cells."

Applicants respectfully disagree. Claim 13 recites a mechanism for reconfiguring a plurality of **intra-processor** information paths **to the array** to respective cells on a periphery of the array. At most, elements 17 and 18 only disclose a means for reconfiguring a plurality of inter-processor communication paths within the array. Applicants respectfully submit that no reasonable interpretation of "intra-processor information paths" would replace "intra-processor" with "inter-processor."

Furthermore, to make this even more abundantly clear, claim 13 is amended to explicitly recite that the mechanism is external to the two-dimensional array – something which elements 17 and 18 are not, and cannot even be modified to be.

Accordingly, for at least these reasons, Applicants respectfully submit that claim 13 is patentable over the cited art.

Claims 15-16

Claims 15-16 depend from claim 13 and are deemed patentable for at least the reasons set forth above with respect to claim 13.

Claims 17-18

Claims 17-18 depend from claim 13. Applicants respectfully submit that Barat does not remedy the shortcomings of Fleck and Roussakov as set forth above with respect to claim 13. Accordingly, claims 17-18 are deemed patentable for at least the reasons set forth above with respect to claim 13.

Claim 20

Among other things, the method of claim 20 includes communicatively connecting the coprocessor to said processor by an interface module having a mechanism for reconfiguring a plurality of information paths between the interface module and respective cells on a periphery of the array.

The Office Action states that Fleck shows the interface module 7, and that Roussakov shows a mechanism for reconfiguring a plurality of information paths between the interface module and respective cells on the periphery of the array as elements 17 and 18.

Even assuming *arguendo* that this was true, it would not produce the method of claim 20. In claim 20, the interface module **includes** the recited mechanism. Meanwhile, in Roussakov elements 17 and 18 are **internal to each processing cell**, and by Roussakov's very operation must inherently remain so. There is no teaching or suggestion that this mechanism could even possibly be removed from the processing cells themselves and somehow transported to the interface module 7 of Fleck. Such a modification of Fleck would seem to be not even possible. Nor does the Office Action even argue that it is, instead arguing that it would have been obvious to substitute Roussakov's array processor in place of the FPGA of Fleck's FIG. 1. But again, as noted above, this would not provide all of the features of claim 1, because the interface module would not include the re cited mechanism, as featured in claim 1.

Accordingly, for at least these reasons, Applicants respectfully submit that claim 20 is patentable over the cited art.

NEW CLAIMS 24-25

New claims 24 and 25 depend respectively from claims 13 and 20 respectively and are deemed patentable for at least the reasons set forth above with respect to claims 13 and 20, and also because of the various novel features recited therein.

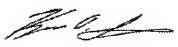
CONCLUSION

In view of the foregoing explanations, Applicants respectfully request that the Examiner reconsider and reexamine the present application, allow claims 1-2, 4-8, 13, 15-18 and 20-25 and pass the application to issue. In the event that there are any outstanding matters remaining in the present application, the Examiner is invited

to contact Kenneth D. Springer (Reg. No. 39,843) at (571) 283.0720 to discuss these matters.

Respectfully submitted,

VOLENTINE & WHITT



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